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Abstract
Much progress has been made in the IC manufacturing. The feature size of 0.13 m, 90 nm 65 nm or below have been the main stream of the IC manufacturing. For the photolithography in the IC process, G-line, I-line, DUV (Deep-Ultra-Violet) and even EUV (Extreme-Ultra-Violet) are used as the light source. Because of the small feature size and the increase in layers, contact holes and ILD (Inter Layer Dielectric) holes make the metal connection hard. The dual damascene process is generally used to overcome this issue. Additionally, Cu process is adopted because the resistivity and electro-migration of Cu are smaller than that of Al. The Cu process replaces the Al process little by little in dual damascene process of 90 nm and become the main process in the manufacture of IC. However, Cu process suffers from the fence and void. In this paper, we propose the investigation of the void in dual damascene process and the hole and trench with large aspect ratios between width and height.
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